Proj_f20_report
EE 421

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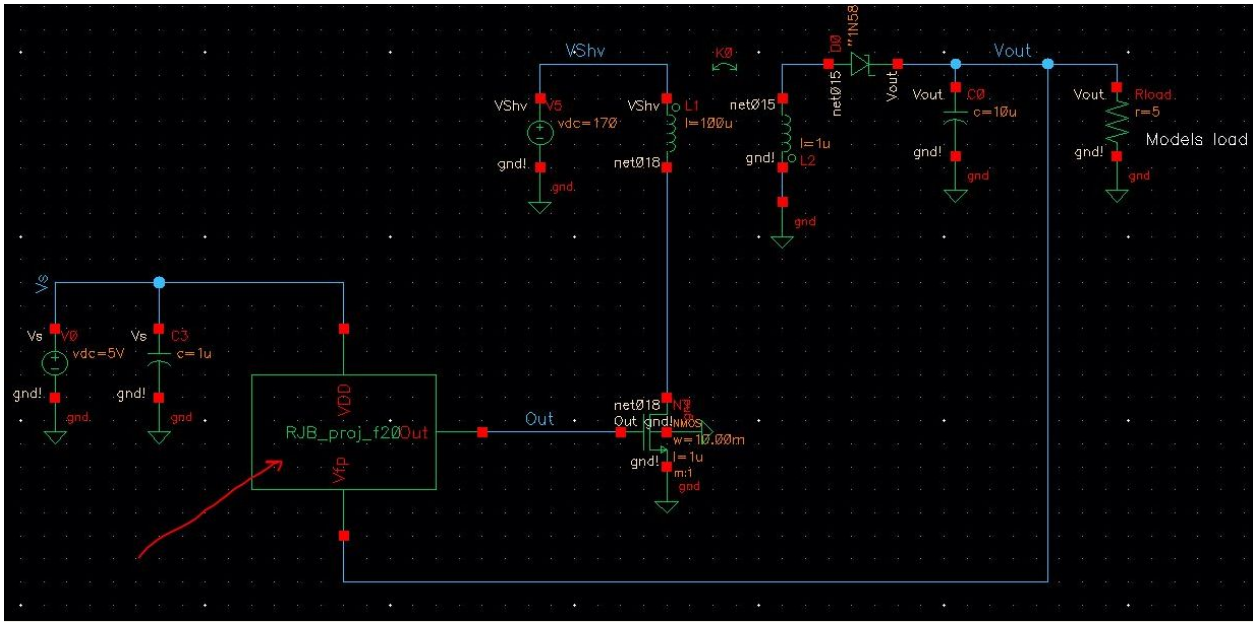
12/04/2020

Controller chip for flyback switching power supply.

The circuit seen below was provided by Dr. Baker of UNLV. Our project was to implement and replace the circuit in the RJB_proj_f20 symbol. When looking at my design the symbol is named DRA_proj_f20 and has the exact same symbol footprint as the one shown here.



What is this Circuit?

This is a flyback switching power supply, it is designed to provide a relatively constant voltage to varied loads. Often, switching power supplies are used to charge our mobile devices, such as laptops, tablets and mobile phones. Switching power supplies are preferred over non-switching power supplies because they are able to do the job with smaller and more economical package sizes. Smaller package sizes are possible with these devices thanks to the higher frequencies they operate at which allows them to utilize very small transformers. This particular design, the flyback switching power supply is most commonly used for phones and tablets thanks to its ability to be implemented in the smallest packages, often not much larger than an inch in any dimension.

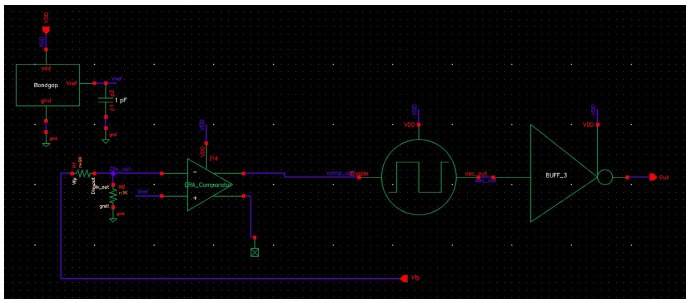
How does this Circuit work?

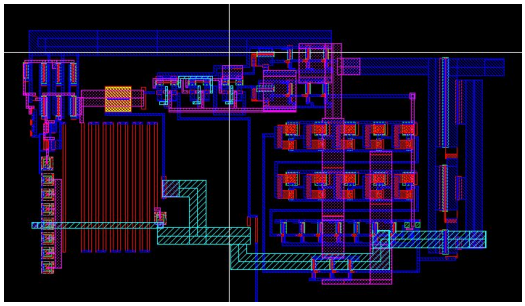
Flyback switching power supplies operate off a feedback loop. This feedback loop operates much like a home ac system, utilizing a desired temperature or voltage in this case, a current temperature or voltage and a difference between those two factors either turns the system on or off. In this case the desired voltage of Vout is 12.5V, this is set in the IC via a bandgap circuit, which outputs a near constant voltage of 1.25V (1/10th our desired output.) By taking the feedback Vout through a 10 to 1 voltage divider, and comparing that to our bandgap

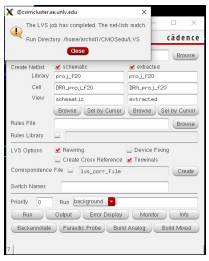
voltage we will know if we want to turn the system on to raise the voltage, or turn it off to lower the voltage.

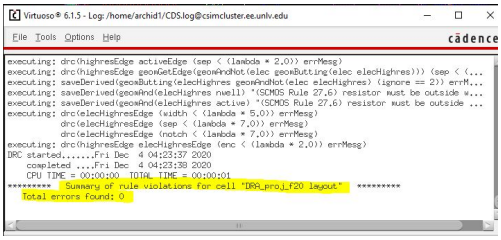
Inside the IC

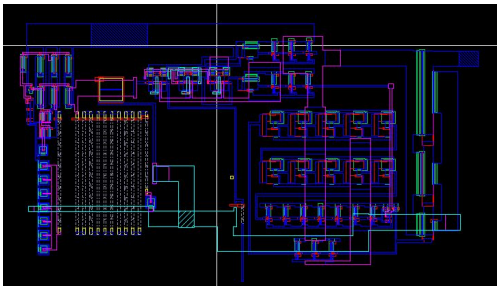
There are 5 major components within the IC, the bandgap, voltage divider, comparator, oscillator and buffer. As explained earlier, the bandgap is used to hold a constant reference voltage that is fed into the comparator along with the feedback voltage (Vout) after going through the voltage divider. The oscillator is used to produce a pulsed signal when the enable is high. This on-off signal is used to create the high frequency switching necessary to use the switching power supply topology, so that a small transformer is able to be used to step the voltage down, in this case the oscillator is running at about 5 MHz. The signal passing from the oscillator to the buffer is important, as this ensures that there is sufficient power available to drive the higher capacitance power mosfet off the chip.





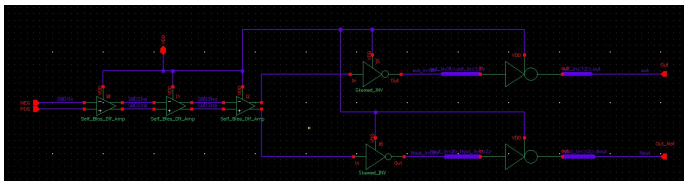






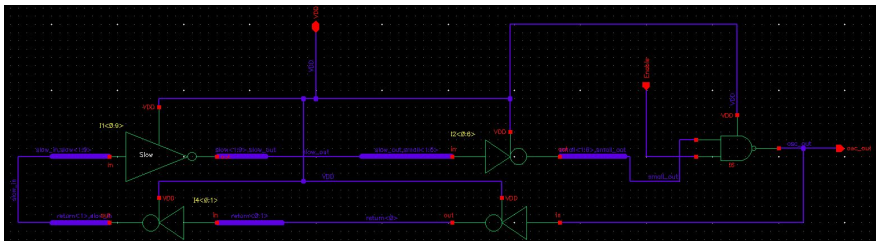
Comparator

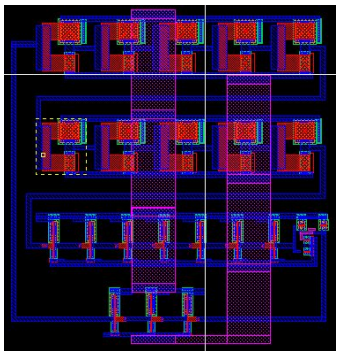
The comparator is made up of three self biased differential amplifiers, two skewed inverters, and four standard inverters. The reason for having three self bias diff amps in series is to increase the sensitivity to differences between the reference voltage and the divided feedback voltage. The high sensitivity is needed to maintain as small a ripple as possible. Skewed inverters after the diff amps is necessary because the output voltage swings from the diff amps aren't a full 5 volts, so the intent behind the skewed inverters is to make the switching point of these inverters right at the middle of the output voltage swing from the diff amps, then the two inverters following the skewed inverter are there to square up the output, making for decisive output logic.



Ring Oscillator

Making up the ring oscillator are three major components, slow inverters, fast inverter, and a NAND gate. When designing a ring oscillator it is important to ensure that there are always an odd number of inversion processes. In this case we have twenty one inversions, ten slow, ten fast and the NAND gate. Having slow inverters makes getting the oscillation slowed down to reasonable levels much less work, and less complex, as using only the quicker, small inverters would require too many inverters to be reasonable.

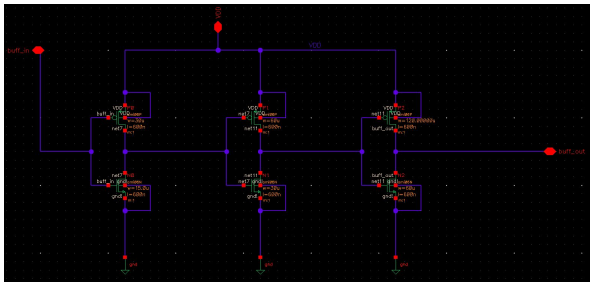


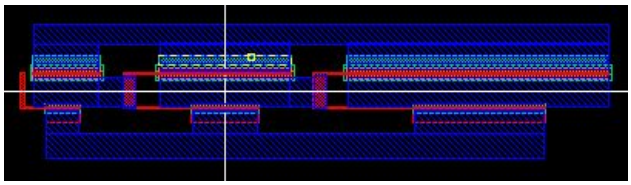


Buffer

Driving the power MOSFET decisively and effectively, requires more current than the typical small inverter used as the output of the NAND gate. Therefore we need a wider mosfet with more current capacity between the NAND and the off chip MOSFET. Choosing the width of the last inverter was done by first determining that the input capacitance of the off chip power MOSFET was near 40pF. That capacitance needed to be driven in a fraction of our oscillators period. As our frequency is near 5MHz, the period is about 200ns, dividing that period by 2, as it is only on for half the period, then dividing by 5, as that is the typical number of time constants used in estimating steady state, gives us a time frame of just 20ns maximum drive time. Given that we have a time constraint, and we know the input capacitance we need to drive, we can divide that time constant by the capacitance to determine an equivalent resistance that would work in this situation. Using the process described we come up with an equivalent resistance of 500 ohms; Noting that an even lower equivalent resistance would be better for driving the off chip capacitance, while increasing the on chip inverters capacitance we can use this 500 ohms as a rough guideline. By taking a typical small inverter and making it 10x wider, we're able to reach an equivalent resistance on both the top and bottom FET's of the inverter of 200 ohms. This is equivalent resistance makes driving the off chip MOSFET very quick, and easy, but requires two supporting mosfets to drive the input of the on chip driving mosfet. These two extra

mosfets add very little delay to the overall hysteresis, so this design should be acceptable, and more versatile in terms of the possible power mosfets it's able to drive.





Descriptive Data:

Steady state:

Table describing the Vout node

Resistance	Ripple[V]	Vout(ave)[V]	I(ave)[A]	Power(output)[W]
1250	0.01	12.52	0.01	0.13
750	0.01	12.52	0.0167	0.21
500	0.01	12.52	0.02504	0.31
250	0.01	12.52	0.0501	0.63
100	0.01	12.52	0.1253	1.57
75	0.01	12.52	0.1669	2.09
50	0.01	12.52	0.2504	3.14
25	0.013	12.52	0.5006	6.27
10	0.102	12.52	1.25	15.65
7.5	0.193	12.47	1.663	20.74
5	0.438	12.4	2.48	30.75
2.5	1.379	11.98	4.792	57.41

Ripple vs Current

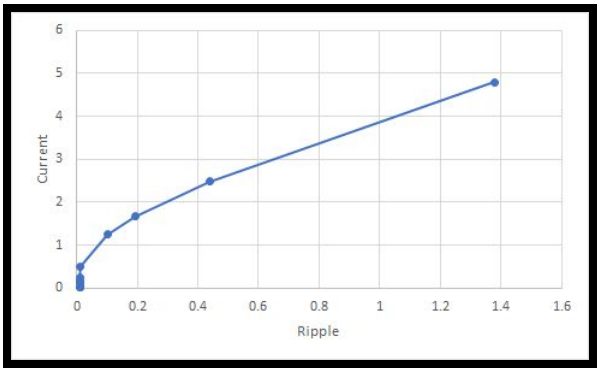


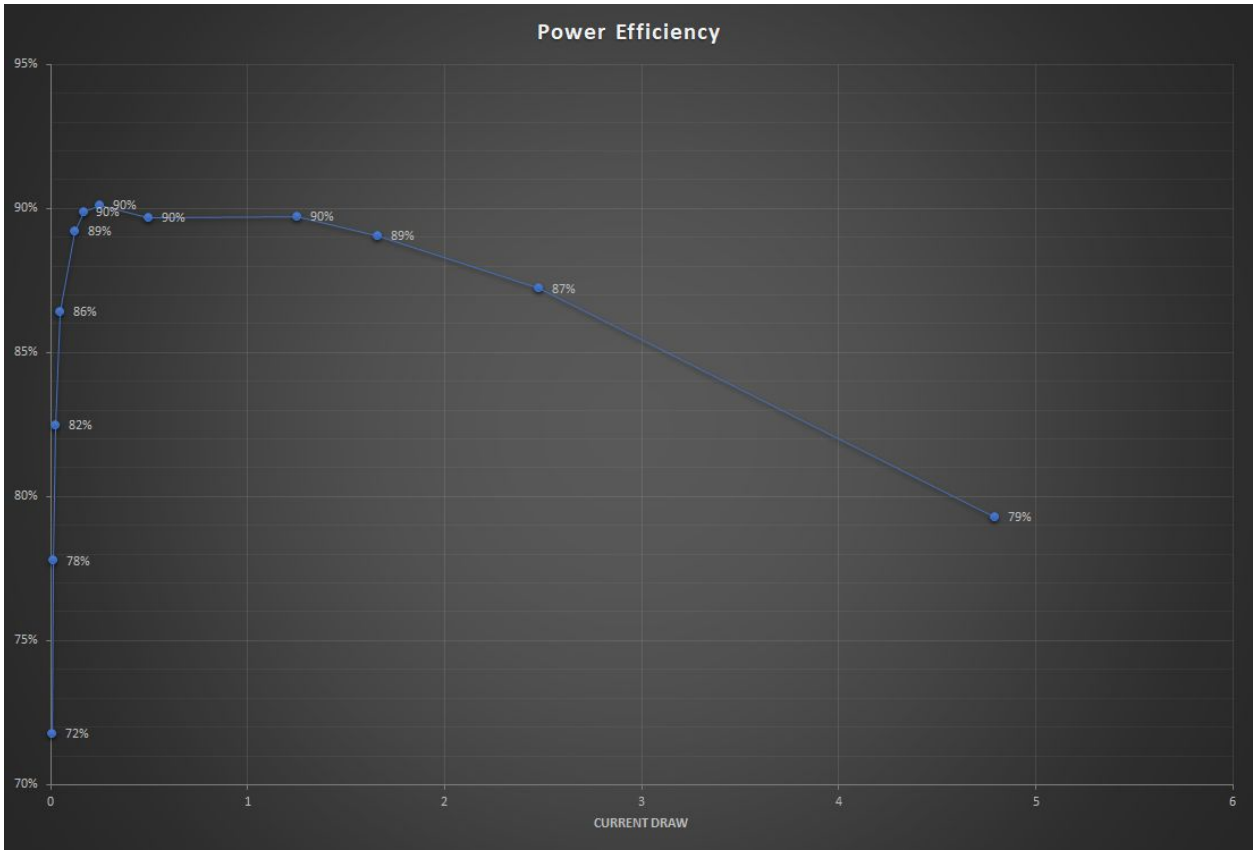
Table describing the VDD node

Resistance	VDD [V]	I(ave) [A]	Power(VDD) [W]
1250	5	0.003977	0.0199
750	5	0.00399	0.0200
500	5	0.004	0.0200
250	5	0.004067	0.0203
100	5	0.004252	0.0213
75	5	0.004333	0.0217
50	5	0.004545	0.0227
25	5	0.00478	0.0239
10	5	0.003685	0.0184
7.5	5	0.003509	0.0175
5	5	0.003378	0.0169
2.5	5	0.003272	0.0164

Table describing Vin or "Vshv" node

Resistance	Vshv [V]	I(ave) [A]	Power(shv) [W]
1250	170	0.000909	0.155
750	170	0.001464	0.249
500	170	0.002118	0.360
250	170	0.00415	0.706
100	170	0.01022	1.737
75	170	0.01355	2.304
50	170	0.02033	3.456
25	170	0.04097	6.965
10	170	0.1025	17.425
7.5	170	0.1369	23.273
5	170	0.2073	35.241
2.5	170	0.4258	72.386

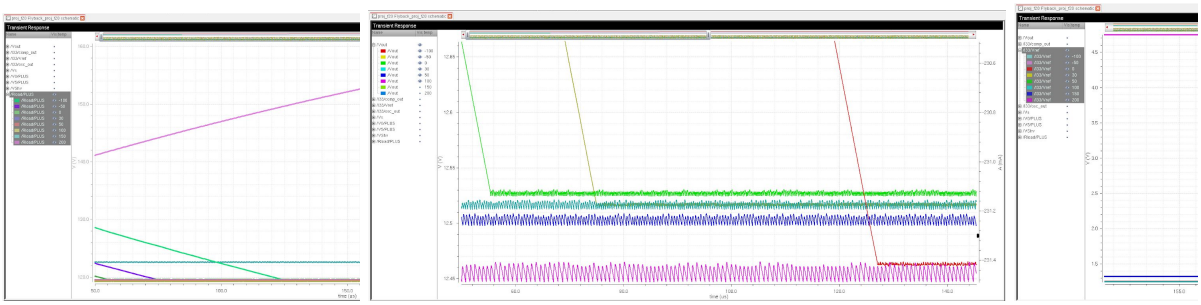
Power Efficiency:



Effective Operating Temp

The following simulations show the effective temperature range of the device. Vout seems to be able to reach near ideal values within 150us for all values between -100C and 100C

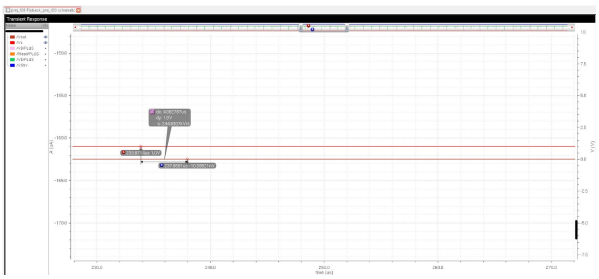
The third picture seems to show that the band gap is largely responsible for inconsistencies above 100C



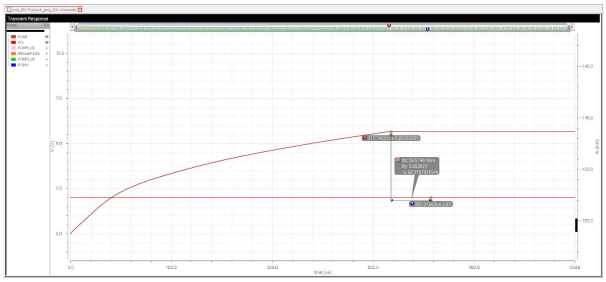
Undervolting the IC

The IC appears to be effective at voltages at or above 4V; 3V and below shows significant degradation of the output voltage.

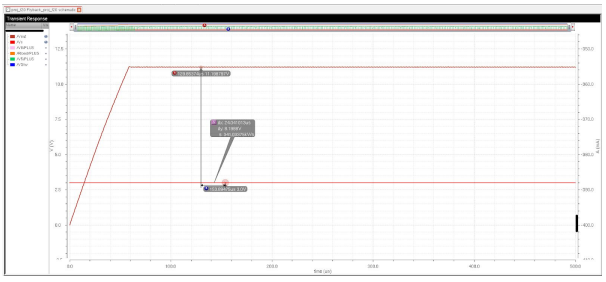
VDD = 1V



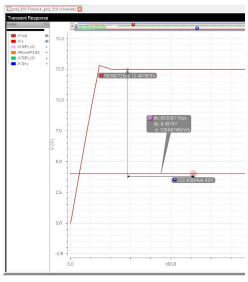
VDD = 2V



VDD = 3V



VDD = 4V



I(Vout)

V(Vout)